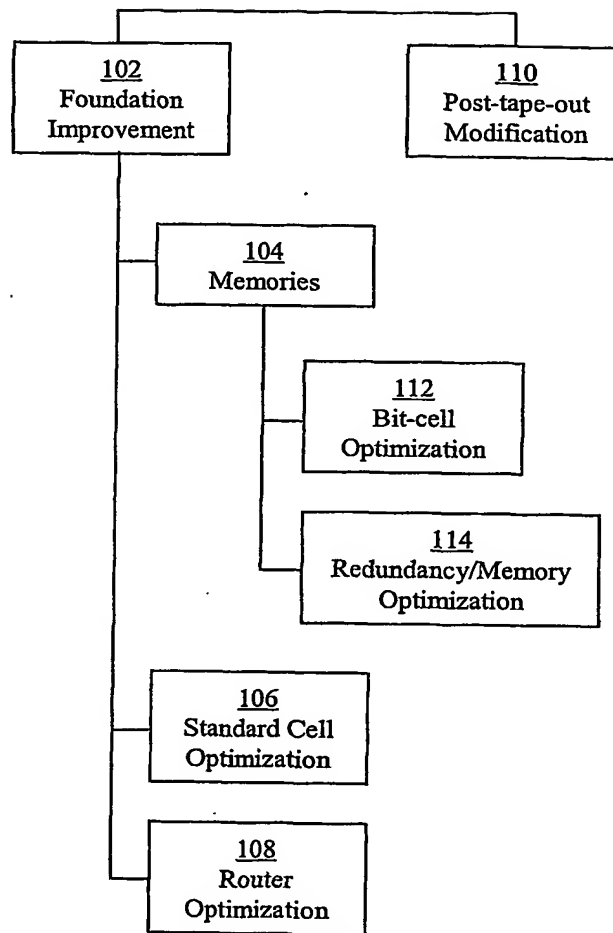
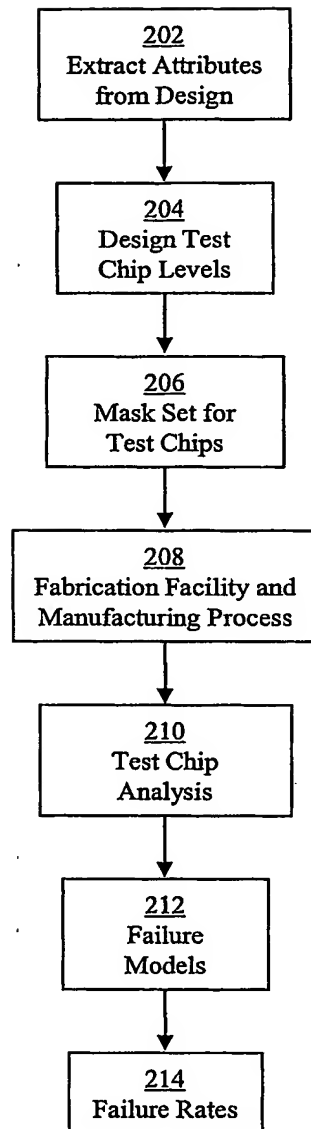


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**FIG. 1: Taxonomy of Design Based Yield Improvements**

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**FIG. 2: Determining "Existing Failure Models"**

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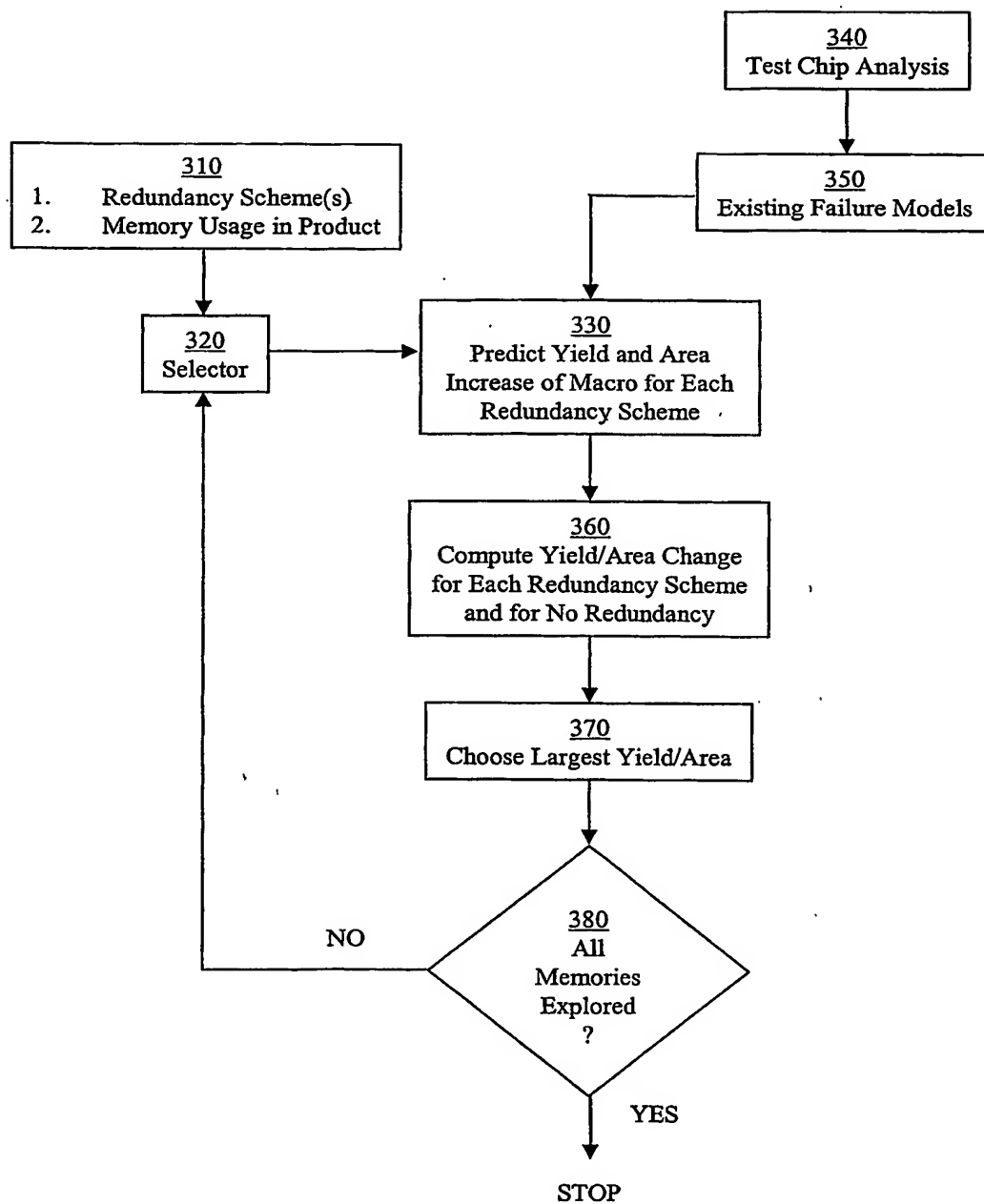


FIG. 3: Bit-Cell Optimization

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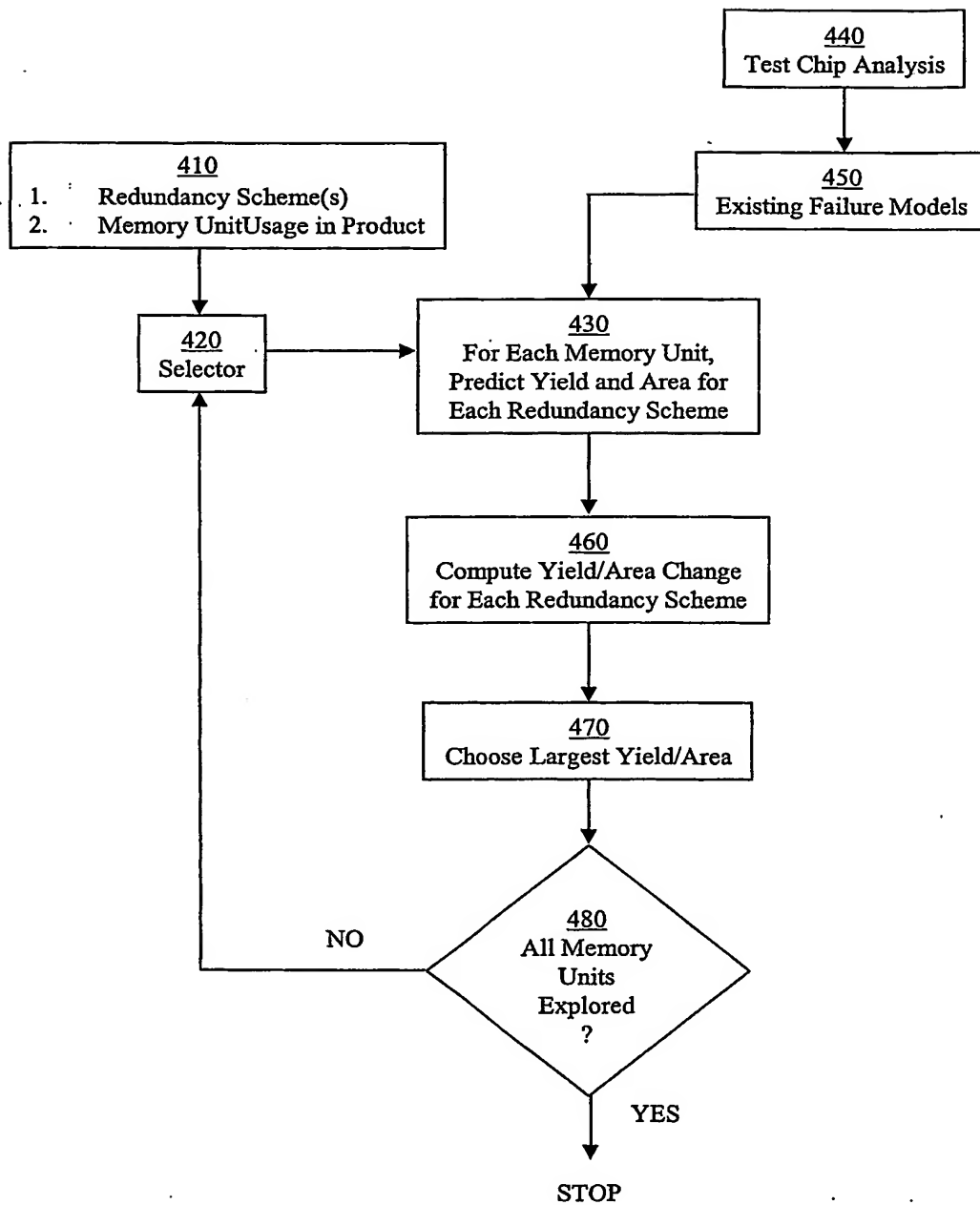


FIG. 4: Redundancy Optimization

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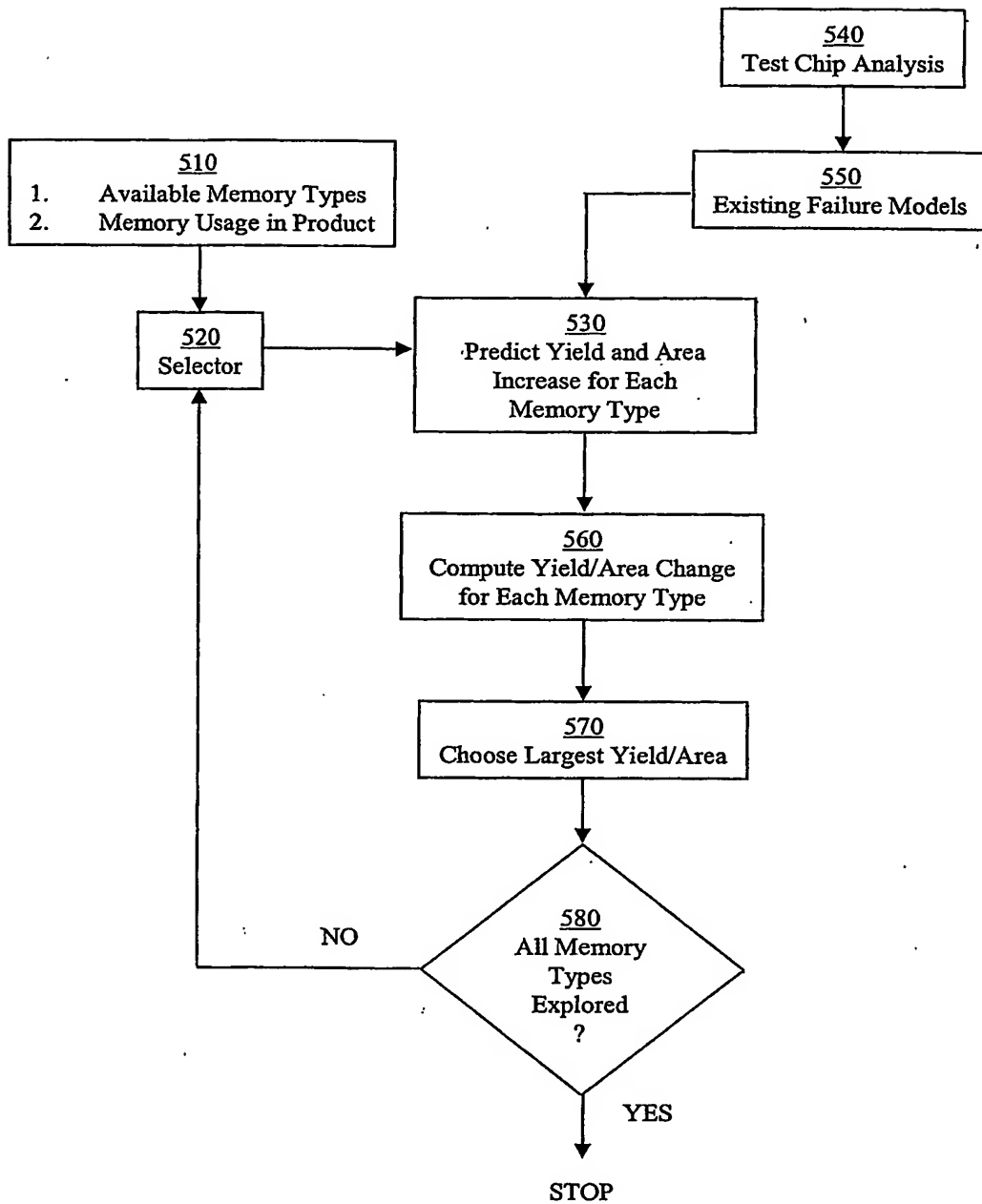


FIG. 5: Memory Type Optimization

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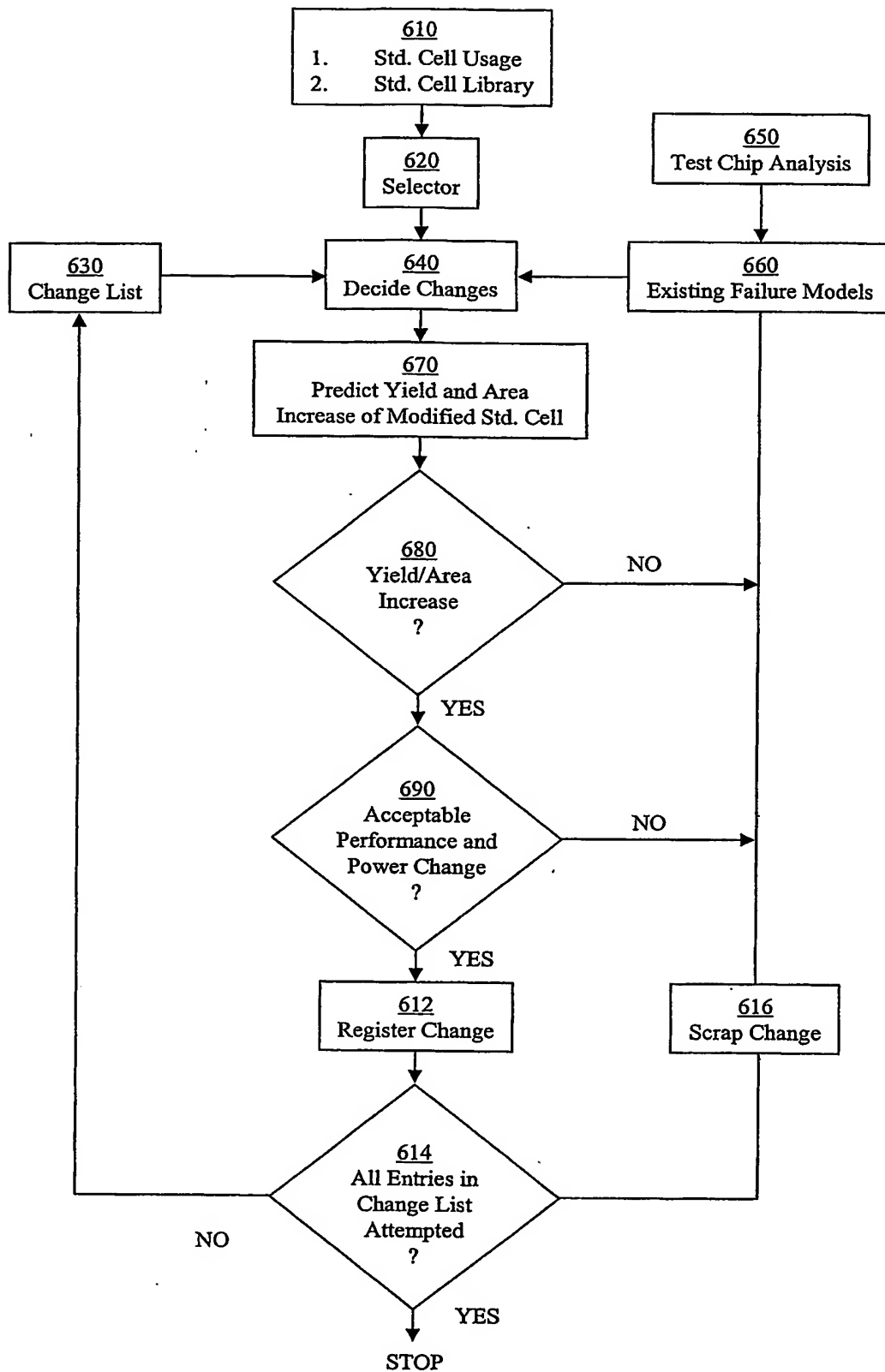


FIG. 6: Standard Cell Optimization

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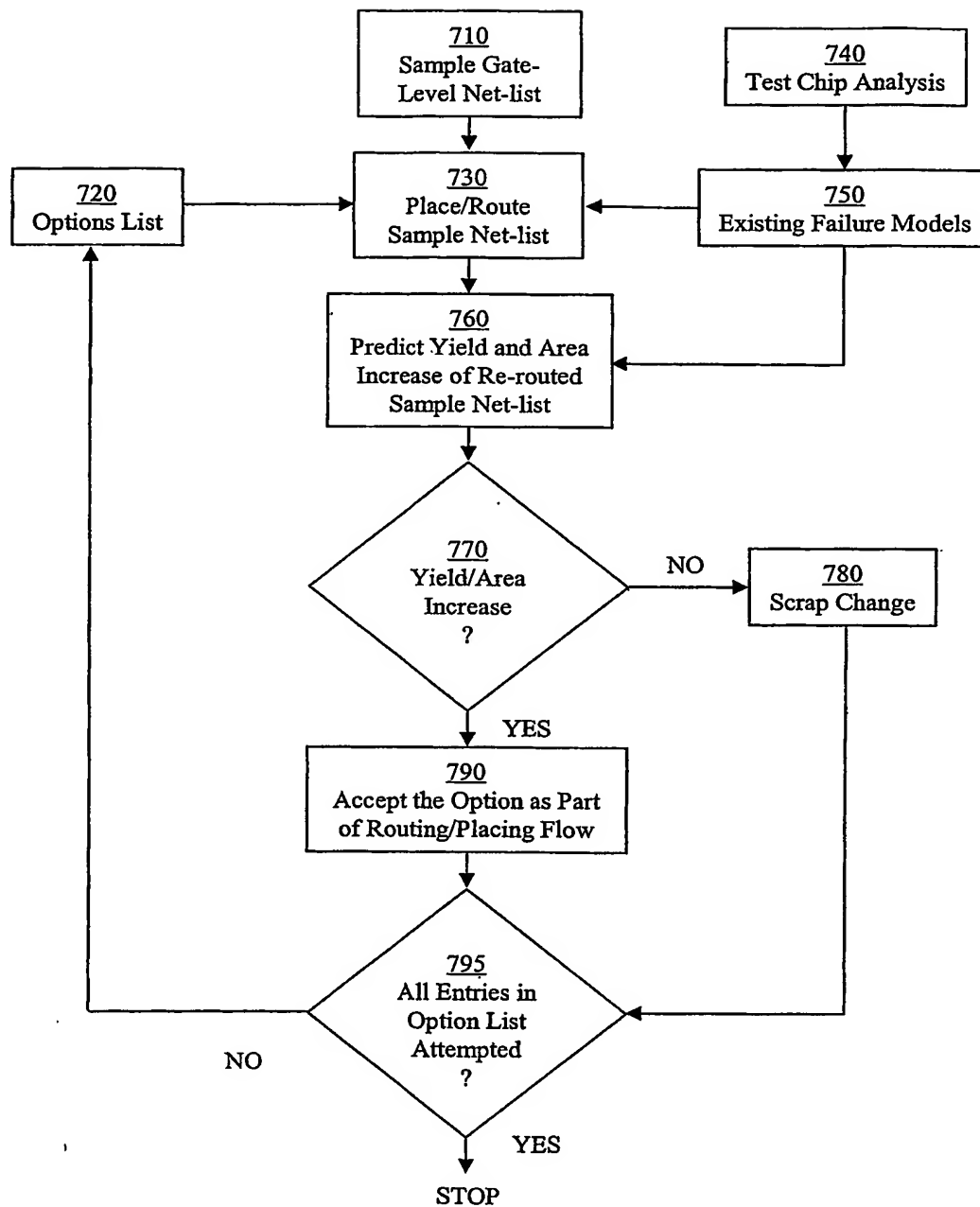
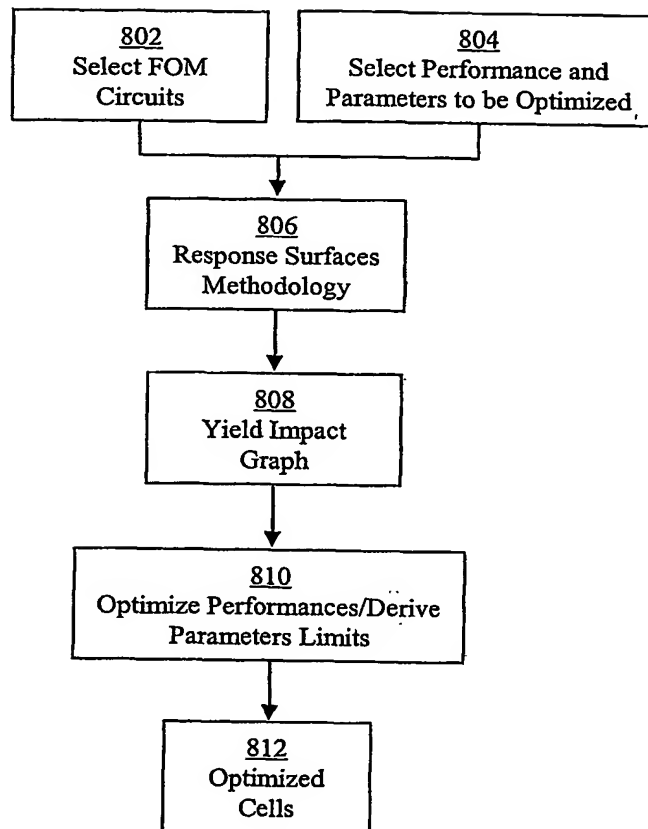


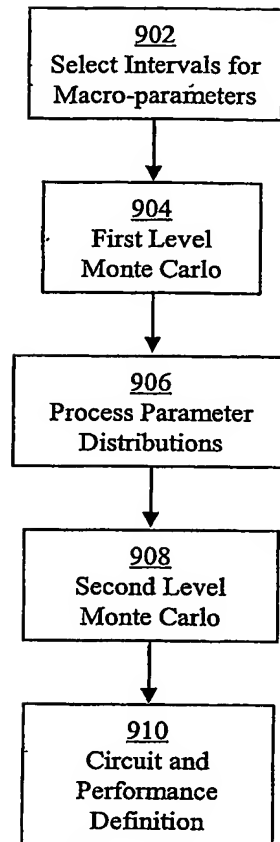
FIG. 7: Router Optimization

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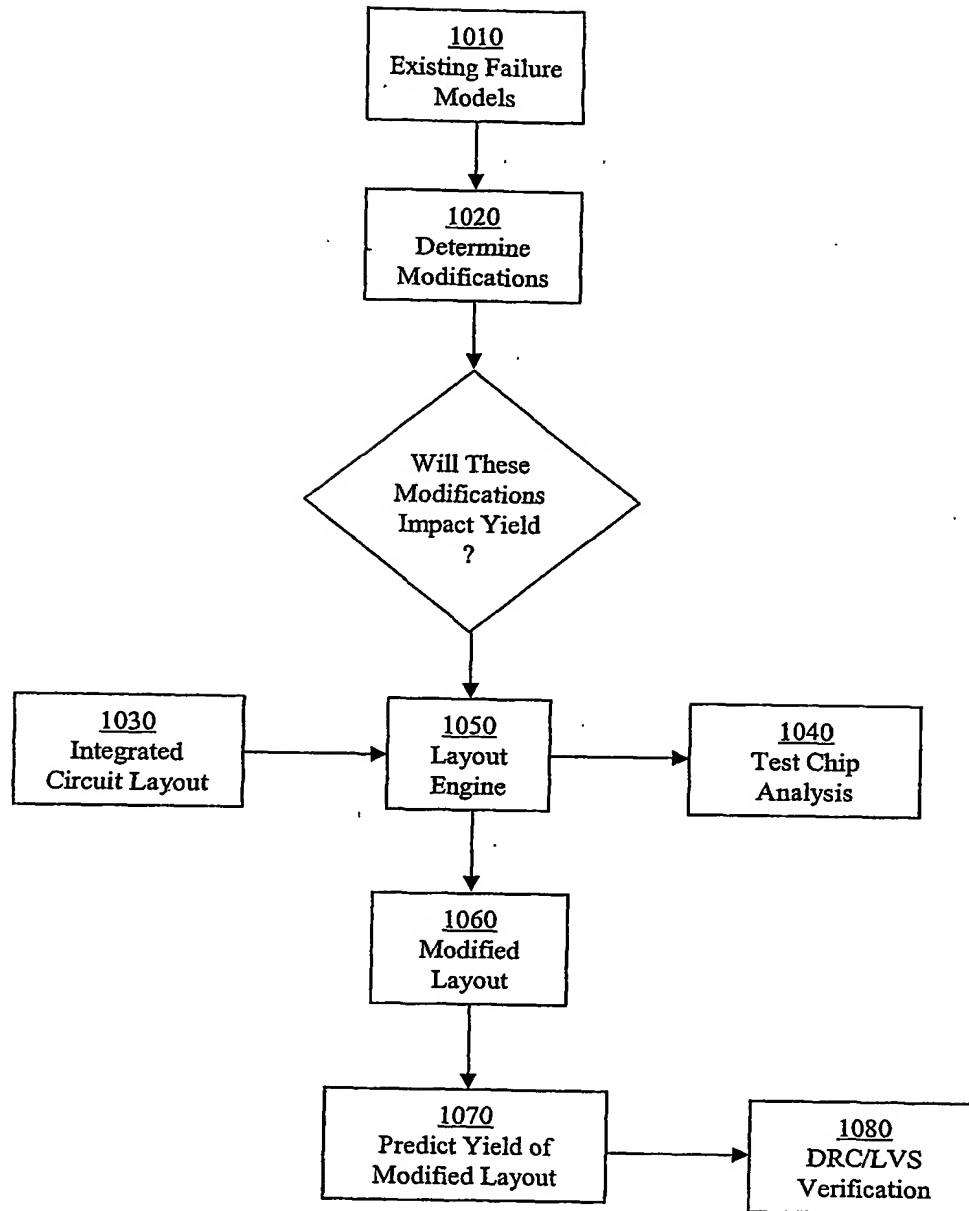
**FIG. 8: Parametric Yield Optimization**



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**FIG. 9: Yield Impact Graph**

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**FIG. 10: Post-tape-out Modification**